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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/809,553	03/25/2004	Charles Ray Johns	AUS920030696US1	7923

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LEE, CHUN KUAN	

ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
10809553	3/25/2004	JOHNS ET AL.	AUS920030696US1

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ART UNIT	**PAPER**
2181	20071102

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Commissioner for Patents

The examiner corrected the Examiner Answer by adding Heading #6.

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/809,553
Filing Date: March 25, 2004
Appellant(s): JOHNS ET AL.

International Business Machines Corporation
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 09/10/2007 appealing from the Office action mailed 03/19/2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US Publication No. 2005/0033874	Futral et al.	Filed: August 5, 2003
US Patent 6,738,881	Ollivier et al.	05-2004
US Patent 6,681,296	Liao et al.	01-2004
US Patent 6,427,201	Ohba	07-2002

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 9, 11, 15 and 16-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Futral et al. (US Pub.: 2005/0033874).

As per claims 1, 9 and 15, Futral teaches a system, a method, and a computer program product having a medium with a computer program embodied thereon to provide software program control of cache management, comprising:

a processor (Fig. 1, ref. 102) and a DMA controller (Fig. 1, ref. 122);

the processor configured to generate DMA commands for the management of a cache (Fig. 1, ref. 116) on the execution of a software program on the processor ([0001], [0011] and [0015]), wherein the processor commands by requesting the DMA controller to transfer data to/from the cache; and

the DMA controller coupled to the processor, configured to execute the DMA commands for the management of a cache ([0001], [0011] and [0015]), wherein the DMA controller implement the transferring of data in accordance to the request from the processor.

As per claims 3, 11 and 16-17, Futral teaches the system, the method, and the computer program product having the medium with the computer program embodied thereon to provide software program control of cache management, comprising:

wherein at least one of the DMA commands is a get command (e.g. to read data from the cache) ([0021]) and

at least one of the DMA commands is a put command (e.g. to store data into the cache) ([0022]).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 7-8, 10, 13-14 and 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Futral et al. (US Pub.: 2005/0033874) in view of Ollivier et al. (US Patent 6,738,881).

Futral teaches all the limitations of claims 1, 9 and 15 as discussed above, where Futral teaches the system, the method, and the computer program product having the medium with the computer program embodied thereon to provide software program control of cache management, comprising wherein the memory (Fig. 1, ref. 116) is coupled to the DMA controller (Fig. 1, ref. 122)

Futral does not teaches the system, the method, and the computer program product having the medium with the computer program embodied thereon to provide software program control of cache management, comprising:

a cache coupled to the DMA controller, the system configured for the execution of the DMA commands for the management of a cache on the DMA controller to manage the operation of the cache coupled to the DMA controller;

wherein the cache is a DMA cache tightly coupled to the DMA controller; and

wherein the cache is a cache for system memory.

Ollivier teaches a system and a method comprising:

implementing a DMA data transferring to and from a plurality of memories (Fig. 2, ref. 220, 222, 224) by utilizing a DMA controller (Fig. 2, ref. 210), wherein the plurality of memories are coupled to the DMA controller and are memories of the system (Fig. 2, ref. 100) (col. 3, l. 57 to col. 4, l. 3); and

the DMA controller further include a plurality of FIFOs (Fig. 3A, ref. FIFO 0, FIFO 1, FIFO 2, FIFO 3, FIFO 4, FIFO 5), wherein the plurality of FIFOs are utilized to manage the data transferring to and from the plurality of memories (Fig. 2, ref. 220, 222, 224) (col. 3, l. 57 to col. 4, l. 3 and col. 5, ll. 39-50).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Ollivier's plurality of memories and plurality of FIFOs into Futral's system of cache management for the benefit of improving the performance of a processor (Ollivier, col. 1, ll. 48-51).

The resulting combination of the references further teaches the system, the method, and the computer program product having the medium with the computer program embodied thereon to provide software program control of cache management, comprising:

the plurality of memory coupled to the DMA controller, wherein the DMA command is executed for transferring data to and from the plurality of FIFOs on the DMA controller, in order to transfer data to and from the plurality of memories coupled to the DMA controller

wherein the plurality of FIFOs (i.e. DMA cache) are tightly coupled to the DMA controller; and

wherein the plurality of memories are the cache for system.

Claims 4-5, 12 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Futral et al. (US Pub.: 2005/0033874) in view of Liao et al. (US Patent 6,681,296).

Futral teaches all the limitations of claims 1, 9 and 15 as discussed above.

Futral does not expressly teach the system, the method, and the computer program product having the medium with the computer program embodied thereon to provide software program control of cache management, comprising:

wherein at least one of the DMA commands is a flush command and

wherein at least one of the DMA commands is a zero command.

Liao teaches a cache management system and method comprising:

a "block flush" command (col. 3, ll. 8-23); and

a "block set to zero" command (i.e. zero command) (col. 3, ll. 8-23).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Liao's "block flush" and "block set to zero" commands into Futral's system of cache management for the benefit of more efficient utilization of on-chip cache (Liao, col. 4, ll. 47-53).

Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Futral et al. (US Pub.: 2005/0033874) in view of Ohba (US Patent 6,427,201).

Futral teaches all the limitations of claim 1 as discussed above, where Futral teaches the system to provide software program control of cache management, comprising wherein the parameters of the DMA commands comprise a transfer size (size 204 of Fig. 2) and a source (Fig. 2, ref. 200) comprises the physical address for the start location (Fig. 2, ref. 210), wherein the size is utilized in defining the physical address for the end location (i.e. effective address low) ([0017] and [0021]), as the effective address is defied by the start location and the end location.

Futral does not expressly teach the system to provide software program control of cache management, comprising wherein the parameters of the DMA commands comprise tag.

Ohba teaches a system and a method comprising a DMA packet including a tag-command (DMA-tag) (Fig. 6 and col. 7, l. 64 to col. 8, l. 3).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Ohba's tag-command into Futral's DMA commands for the benefit of providing an information processing device for efficiently performing various processing operations (Ohba, col. 1, ll. 58-63). The resulting combination of the references further teaches the system to provide software program control of cache management, comprising wherein the parameters of the DMA commands comprise tag-command, size and end location of the physical address.

(10) Response to Argument

I. Claims 1, 3, 9, 11 and 15-17

Issue 1

Appellant argued that Futral fail to teach or suggest DMA command for management of a cache, because the word "cache" does not appear anywhere in the Futral reference to indicate Futral's memory, reference number 16 of figure 1, is a "cache." Additionally, in accordance to Appellants' own definition of cache, Futral's memory is a slower storage not a cache, and if Futral's memory were a cache, then Futral would call it a "cache."

Examiner's Response to Issue

In accordance to Appellant's own definition of a cache "[a] cache is a storage that keeps frequently accessed data or program instructions readily available so that the device, in this case a DMA controller, does not access them repeatedly from a slower storage." Additionally, in accordance to Appellant's

disclosure, in the Abstract of the application, "a cache can be a system cache or a DMA cache."

The examiner respectfully disagree and maintains that Futral's teaching of a memory in a computer system does allow for frequent and rapid access of data in a fashion substantially similar to the Appellant's claim language regarding a cache. Both the Appellant's language and Futral's memory teach the access of data via memory. Furthermore, the definition of a cache is considered among other things a system memory and therefore Futral's memory, which is directly related to a computer system, reads on applicant's claimed language.

Issue 2

The Appellant argued that Futral teaches a processor issuing DMA commands to a DMA controller to perform DMA operation, rather than to perform the claimed "cache management" operation.

Examiner's Response to Issue

The examiner respectfully disagrees and maintains that Futral's the DMA operation to be associated with cache management operation, such as management the data transferring operation to/from the cache. Therefore, Futral does teach a DMA controller that is configured to execute the DMA commands for the management of a cache.

II. Claims 2, 7, 8, 10, 13, 14, 20 and 21

Issue

Appellant argued that like Futral, Ollivier fails to teach or suggest a cache or a DMA controller configured to execute DMA command for cache management; therefore neither Futral nor Ollivier teaches or suggests a cache or a DMA controller that is configured to execute DMA commands for cache management.

Examiner's Response to Issue

The examiner respectfully disagrees, as the examiner explained in detail above, the examiner relies on Futral's teachings, and not on Ollivier's teaches, to read on Appellant's claimed "cache" and "cache management" operation.

III. Claims 4, 5, 12, 18 and 19

Issue

Appellant argued Liao fails to teach or suggest providing DMA commands for cache management or a DMA controller that is configured to execute DMA commands for cache management, and Futral also fails to teach or suggest a DMA controller that is configure to execute a DMA command for cache management.

Examiner's Response to Issue

The examiner respectfully disagrees, the examiner is relying on Futral to teach the claimed providing "DMA command" for cache management;

furthermore, as explained in detail above, the examiner relies on Futral's teachings, and not on Liao's teaches, to read on Appellant's claimed "DMA controller ... configure to execute the DMA commands for cache management".

IV. Claim 6

Issue

Appellant argued Ohba fails to teach or suggest providing DMA commands for cache management or a DMA controller that is configured to execute DMA commands for cache management, and Futral also fails to teach or suggest a DMA controller that is configure to execute a DMA command for cache management.

Examiner's Response to Issue

The examiner respectfully disagrees, the examiner is relying on Futral to teach the claimed providing "DMA command" for cache management; furthermore, as explained in detail above, the examiner relies on Futral's teachings, and not on Ohba's teaches, to read on Appellant's claimed "DMA controller ... configure to execute the DMA commands for cache management".

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Chun-Kuan Lee
Patent Examiner
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